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UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE

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METHOD AND SYSTEM FOR PROVIDING HALO IMPLANT TO A SEMICONDUCTOR DEVICE WITH MINIMAL IMPACT TO THE JUNCTION CAPACITANCE

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and more particularly providing a halo implant when manufacturing semiconductor devices.

BACKGROUND OF THE INVENTION

A halo implant is typically utilized to implant dopant on a semiconductor device. In-line lithography or DUV (deep ultra violet) photoresist is typically utilized to mask the halo implant process. Typically, the same mask (lightly doped drain) (LDD) is utilized for the halo implant, since the halo implant takes place after the LDD implant. Due to the chemistry of the photoresist, an implant shadowing problem oftentimes occurs utilizing conventional processes (mask & photoresist set), which adversely affects yield and performance of the devices as manufacturing processes move toward smaller geometries.

The first problem is that the photoresist thickness in the area of implant is of a thickness such that an implant delivered at a 45° angle can result in an asymmetric and leaky transistor. A second problem is the thickness of the photoresist related to the trench oxidation region of the device. Accordingly, if a thick photoresist (0.55μm or greater) is placed over the trench oxidation, due to the soft jelly type nature of the photoresist oftentimes the photoresist will fall and cover areas that are to be implanted. Even if the photoresist stands erect at the smaller process technologies, the halo implant will not reach the targeted areas. In addition, the conventional processes do not typically account for the need for selective doping of the source/drain area.

Accordingly, what is needed is a system and method for overcoming the above-identified problems at smaller process geometrics. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A method and system for providing a halo implant to a semiconductor device is disclosed. The method and system comprises providing a thin photoresist layer to the semiconductor device. The method and system further includes providing the halo implant to the appropriate area of the semiconductor device.

Accordingly, in a system and method in accordance with the present invention, a photo photoresist that is capable of thinner profile, i.e., DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows. With this photoresist thickness, taking into account other height variables, the source and drain regions can be opened only as needed.

At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.

In the smaller geometries of 0.18 um technologies and lower, the gate height will actually work to advantage and help reduce unwanted counter doping of the source/drain area. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries.

Accordingly, the process in accordance with the present invention is the improvement in the manufacture-ability as well as enhancing the process capability and device performance and speed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow chart illustrating a conventional process for providing a halo implant.

Figure 2 is a diagram illustrating the semiconductor device after a conventional halo implant.

Figure 3 is a flow chart of a system in accordance with the present invention.

Figure 4 is a diagram illustrating a semiconductor device after a halo implant in accordance with the present invention.

DETAILED DESCRIPTION

The present invention relates to semiconductor devices and more particularly providing a halo implant when manufacturing semiconductor devices. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Figure 1 is a flow chart illustrating a conventional process for providing a halo implant. Typically in the conventional process, first a thick photoresist is provided, via step 102. Then,

an LDD implant is provided, via step 104. The thick photoresist or LDD mask in a conventional process is typically a photoresist that is 0.55μm in height. After the LDD implant is provided, then we provide what is referred to as the halo implant, via step 106. The halo implant typically is provided at a 45° angle to implant underneath the gate area. For a wafer at a 45° implant, to consistently implant the intended area, a LDD mask is utilized which does not cover the source or drain regions.

Figure 2 is a diagram illustrating the semiconductor device 200 after a conventional halo implant. Accordingly oftentimes the halo implant 202 ends up providing dopant to all of the source region 204 and drain region 206. Since only the area directly underneath the gate 208 is the area of interest for the implant, there is leakage and other problems associated therewith. Accordingly, the entire active area 212 is open primarily because the thickness of the photoresist mask 212 is such that at a 45° angle, the ultraviolet rays cannot accurately be provided underneath the gate area.

As is seen, with a photoresist mask 212 thickness of .5μm, the 45° angle will require that a large portion of the ultraviolet radiation will not reach the area of interest because at that angle, with the thick photoresist, it is not possible. In addition, if a thick photoresist of (0.5μm or greater) is placed over the trench oxidation 207, due to the soft jelly type nature of the photoresist, oftentimes the photoresist will fall over in the trench oxidation area and cover areas that are to be implanted. Even if the photoresist stands erect at the smaller process technologies, the halo implant will not reach the targeted areas.

In a system and method in accordance with the present invention, the implant area is selectively targeted instead of performing a blanket implant. This is accomplished by using a thinner photoresist mask thickness of between 0.1 μm to 0.2 μm instead of 0.55 μm to 0.8 μm

photoresist utilized in the conventional process. To more particularly describe the features of the present invention, refer now to the following discussion in conjunction with the figures.

Figure 3 is a flow chart of a system in accordance with the present invention. Typically as in the conventional process, first a thick photoresist is provided, via step 302. Then, an LDD implant is provided, via step 304. Next, the thick photoresist is removed, via step 306. Thereafter, a thin photoresist is provided, via step 308. Thereafter, a halo implant is provided, via step 310. The halo implant typically is provided at a 45° angle to implant underneath the gate area. For a wafer at a 45° halo implant, to consistently implant the intended area, a LDD mask is utilized which does cover a substantial portion of the source or drain regions.

Figure 4 is a diagram illustrating a semiconductor device 400 after a halo implant in accordance with the present invention. As is shown, the photoresist mask 402 is a smaller height (.1μm to .2μm) than in the conventional process, which allows for more of the source and drain regions 404 and 406 respectively to be masked by the photoresist 402.

Accordingly, in a system and method in accordance with the present invention, a photoresist that is capable of thinner profile, i.e., a DUV photoresist is utilized. This will allow one to lower the photoresist thickness to the proposed 1000A (in the field) or lower if the process allows. With this photoresist thickness, taking into account other height, the source and drain regions can be opened only as needed. At a 45° angle, the implant can be delivered to all transistors in the circuit in the targeted area as well as getting only a large amount of the dose (up to ¾ of the dose) to the transistor edge which sits on the trench edge. This will also minimize the counter doping of the source drain with the opposite species as is required by the definition of the halo process.

In the smaller geometries of 0.18 um technologies and lower, the gate height will

actually work to advantage and help reduce unwanted counter doping of the source and drain region. In this way the counter doping can be maintained to an absolute minimum. The final advantage is that with the thinner photoresist, we will enhance our ability to provide the implant to smaller geometries. Accordingly, the process in accordance with the present invention is the improvement in the manufacture-ability as well as enhancing the process capability and device performance and speed.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one or ordinary skill in the art without departing from the spirit and scope of the appended claims.